WHAT IS CLAIMED IS:

1. A fused Booth encoder multiplexer logic cell comprising:

a logic circuit having a plurality of operand input bits including multiplier input bits and multiplicand input bits, and an output node which produces a single partial product bit according to a Boolean function of said plurality of operand input bits based on a Booth encoding and selection algorithm.

2. A fused Booth encoder multiplexer utilizing a plurality of fused Booth encoder multiplexer logic cells according to Claim 1, wherein:

the logic cells are arranged in a two-dimensional array on an integrated circuit and operate in parallel to produce a respective plurality of partial product bits; and

a given one of the logic cells has a unique set of multiplicand and multiplier input bits.

3. The fused Booth encoder multiplexer logic cell of Claim 1 wherein:

the operand inputs bits include two multiplicand input bits A(i..i+1) and three multiplier input bits C(i-1..i+1); and

the Boolean function which produces the single partial product bit is given by the expression

$$S = (A(i) \oplus C(i-1)) \cdot (C(i) \oplus C(i+1)) + A(i+1) \cdot \overline{C(i-1)} \cdot C(i) \cdot C(i+1) + \overline{A(i+1)} \cdot C(i-1) \cdot \overline{C(i)} \cdot \overline{C(i+1)}.$$

4. The fused Booth encoder multiplexer logic cell of Claim 1 wherein the logic circuit includes:

a clock input;

a logic tree containing a plurality of logic transistors controlled respectively by said plurality of operand bit inputs and interconnected to carry out the

Boolean function to produce a value for a multiplication operation at a dynamic node;

a power transistor coupling said logic tree to a voltage source, said power transistor being controlled by said clock input;

a foot transistor coupling said logic tree to electrical ground, said foot transistor being controlled by said clock input; and

a latch connected to said dynamic node which maintains the value at said output node, said latch being controlled by said clock input.

5. The fused Booth encoder multiplexer logic cell of Claim 4 wherein said latch includes:

a first P-MOS transistor having a drain connected to said dynamic node, a source connected to said voltage source, and a gate;

a second P-MOS transistor having a gate connected to said dynamic node, a source connected to said voltage source, and a drain connected to said gate of said first P-MOS transistor and said output node; and

an N-MOS transistor having a gate connected to said dynamic node, a source connected to said drain of said second P-MOS transistor, said gate of said first P-MOS transistor and said output node, and a drain connected to electrical ground.

6. The fused Booth encoder multiplexer logic cell of Claim 4 wherein said latch includes:

a first P-MOS transistor having a gate connected to said dynamic node, a source connected to said voltage source, and a drain;

a second P-MOS transistor having a gate, a source connected to said voltage source, and a drain connected to said drain of said first P-MOS transistor;

a first N-MOS transistor having a gate connected to said dynamic node, a source connected to said drains of said first and second P-MOS transistors, and a drain;

a second N-MOS transistor having a gate connected to said clock input, a source connected to said drain of said first N-MOS transistor, and a drain connected to electrical ground;

a third N-MOS transistor having a gate, a source connected to said drain of said first N-MOS transistor, and a drain connected to electrical ground; and

an inverter having an input connected to said drains of said first and second P-MOS transistors, and an output connected to said gates of said first P-MOS transistor and said third N-MOS transistor, said inverter output being further connected to said output node to produce an inverted value.

7. The fused Booth encoder multiplexer logic cell of Claim 6 wherein said first P-MOS transistor and said first N-MOS transistor invert the value from the dynamic node, and the Boolean function of said logic tree accounts for inversion of the value by said first P-MOS transistor and said first N-MOS transistor.

8. The fused Booth encoder multiplexer logic cell of Claim 4 wherein said logic tree includes a plurality of transistor stacks, each transistor stack having a plurality of said logic transistors serially connected source-to-drain, with one logic transistor in each stack having a source connected to said drain of power transistor and said dynamic node, and another logic transistor in each stack having a drain connected to said source of said foot transistor.

9. The fused Booth encoder multiplexer logic cell of Claim 8 wherein a first source/drain junction in a first one of said transistor stacks is connected to a second source/drain junction in a second one of said transistor stacks.

10. The fused Booth encoder multiplexer logic cell of Claim 8 wherein said operand bit inputs include a plurality of multiplicand bit inputs and a plurality of multiplier bit inputs, and a given one of said transistor stacks includes:

a first logic transistor having a gate controlled by one of said multiplicand bit inputs;

a second logic transistor having a gate controlled by a first one of said multiplier bit inputs;

a third logic transistor having a gate controlled by a second one of said multiplier bit inputs; and

a fourth logic transistor having a gate controlled by a third one of said multiplier bit inputs.

11. A multiplier circuit comprising:

a fused Booth encoder multiplexer unit which uses two input operands to produce a plurality of partial product bits for a multiplication operation;

a tree unit which uses the partial product bits to generate a plurality of partial products; and

an adder unit which uses the partial products to generate intermediate sum and carry results for the multiplication operation.

12. The multiplier circuit of Claim 11 wherein:

said two input operands include a multiplicand and a multiplier, each having a plurality of bits; and

said fused Booth encoder multiplexer unit is laid out on an integrated circuit chip with a plurality of generally parallel multiplicand input bit wires, and a plurality of generally parallel multiplier input bit wires, said multiplicand input bit wires further being arranged generally orthogonal to said multiplier input bit wires and overlying said multiplier input bit wires.

13. The multiplier circuit of Claim 11 wherein said fused Booth encoder multiplexer unit has a plurality of encoder-selector cells each having a logic tree containing a plurality of logic transistors controlled by a respective plurality of operand bit inputs and interconnected to carry out a Boolean function according to a Booth encoding and selection algorithm to produce a partial product bit for a multiplication operation at a dynamic node, and a latch connected to said dynamic node which maintains the value at an output node.

14. The multiplier circuit of Claim 13 wherein a given one of said logic trees includes a plurality of transistor stacks, each transistor stack having a plurality of said logic transistors serially connected source-to-drain, with one logic transistor in each stack having a source connected to said drain of power transistor and said dynamic node, and

another logic transistor in each stack having a drain connected to said source of said foot transistor.

15. The multiplier circuit of Claim 13 wherein said encoder-selector cells operate in parallel to produce the plurality of the partial product bits.

16. A arithmetic logic unit comprising:

first, second and third operand inputs;

an exponent calculator which calculates an intermediate exponent from a sum of operand exponent portions from said operand inputs;

a multiplier which calculates intermediate sum and carry results based on operand mantissa portions from first and second ones of said operand inputs, said multiplier having a fused Booth encoder selector;

an alignment shifter which produces a shifted mantissa using an operand mantissa portion from a third one of said operand inputs based on the intermediate exponent;

an adder/incrementer which uses the intermediate sum and carry results and the shifted mantissa to produce a final mantissa; and

an exponent adder which combines the final mantissa with the intermediate exponent to produce a final result.

17. The arithmetic logic unit of Claim 16 wherein said fused Booth encoder selector has a plurality of encoder-selector cells which operate in parallel to produce a plurality of partial product bits.

18. The arithmetic logic unit of Claim 17 wherein each of said encoder-selector cells utilizes a limiting switching dynamic logic circuit.

19. The arithmetic logic unit of Claim 17 wherein each of said encoder-selector cells utilizes a domino circuit.

20. The arithmetic logic unit of Claim 17 wherein said multiplier further has a Wallace tree which collects the partial product bits to generate a plurality of partial products.

21. The arithmetic logic unit of Claim 20 wherein said multiplier further has a ripple carry adder which combines the partial products to produce the intermediate sum and carry results.

22. A logic circuit for a fused Booth encoder multiplexer logic cell, comprising:

two multiplicand inputs A(i..i+1);

three multiplier inputs C(i-1..i+1);

an output node; and

a plurality of interconnected transistors controlled by said multiplicand and multiplier inputs, respectively, said transistors producing a value at said output node such that:

the value is the first multiplicand input A(i) when the first multiplier input C(i-1) is on and when only one of the second and third multiplier inputs C(i..i+1) is on;

the value is the complement $\overline{A(i)}$ of the first multiplicand input when the first multiplier input C(i-1) is off and when only one of the second and third multiplier inputs C(i..i+1) is on;

the value is the second multiplicand input A(i+1) when the first multiplier input C(i-1) is off and when both of the second and third multiplier inputs C(i..i+1) are on;

the value is the complement $\overline{A(i+1)}$ of the second multiplicand input when the first multiplier input C(i-1) is on and both of the second and third multiplier inputs C(i..i+1) are off; and

the value is off when the multiplier bits C(i-1..i+1) are either all on or all off.